What is claimed is:

1. An inductor in an integrated circuit, comprising:

a conductive trace disposed over an insulating layer, said insulating layer overlying a semiconductor substrate of a first conductivity type; and

at least two deep wells of opposite conductivity type in said substrate underneath said track.

2. The inductor of claim 1 wherein said conductive trace comprises metal.

3. The inductor of claim 1 wherein said semiconductor substrate is a p-type substrate and said deep wells are n-type wells

4. The inductor of claim 1 wherein said semiconductor substrate is an n-type substrate and said deep wells are p-type wells.

5. The inductor of claim 1 wherein said deep wells are not reverse biased.

6. The inductor of claim 1 wherein said deep wells are arranged in a pattern to form a substantial depletion space in said substrate underneath said trace.

7. The inductor of claim 1 wherein said deep wells are cuboid.

8. The inductor of claim 1 wherein said deep wells are L shaped cuboid.

9. The inductor of claim 1 wherein said deep wells are continuous.

10. The inductor of claim 9 wherein said deep wells are continuous for at least 1.5 μm approximately from a surface of said substrate underneath said insulating layer.

11. The inductor of claim 1 wherein said deep wells are formed by ion implantation.

12. The inductor of claim 11 wherein said ion implantation comprises a first stage in which ions are accelerated to a first energy level and at least a second stage in which ions are accelerated to an energy level different from said first energy level.

13. An inductor in an integrated circuit, comprising:

a conductive trace disposed over an insulating layer, said insulating layer overlying a semiconductor substrate of a first conductivity type;

a shallow trench isolation region, formed in said substrate underneath said trace; and

at least two deep wells of opposite conductivity type in said substrate underneath said shallow trench isolation region.

14. The inductor of claim 13 wherein said conductive trace comprises metal.

15. The inductor of claim 13 wherein said shallow trench isolation comprises silicon dioxide.

16. The inductor of claim 13 wherein said semiconductor substrate is a p-type substrate and said deep wells are n-type wells.

17. The inductor of claim 13 wherein said semiconductor substrate is an n-type substrate and said deep wells are p-type wells.

18. The inductor of claim 13 wherein said deep wells are not reverse biased.

19. The inductor of claim 13 wherein said deep wells are arranged in a pattern to form a substantial depletion space in said substrate underneath said trace.

20. The inductor of claim 13 wherein said deep wells are cuboid.

21. The inductor of claim 13 wherein said deep wells are L shaped cuboid.

22. The inductor of claim 13 wherein said deep wells are continuous.

23. The inductor of claim 22 wherein said deep wells are continuous for at least 1.5 μm approximately from a plane in said substrate underneath and adjacent to said shallow trench isolation region.

24. The inductor of claim 13 wherein said deep wells are formed by ion implantation.

25. The inductor of claim 24 wherein said ion implantation comprises a first stage in which ions are accelerated to a first energy level and at least a second stage in which ions are accelerated to an energy level different from said first energy level.

26. A method of manufacturing an inductor on an integrated circuit, comprising:
providing a semiconductor substrate of a first conductivity type;
forming at least two deep wells of opposite conductivity type in said substrate;
forming an insulation layer over said substrate; and
forming a conductive trace over said insulating layer.

27. The method of claim 26 wherein said deep wells are arranged in a pattern to form a substantial depletion space in said substrate underneath said trace.

28. The method of claim 26 wherein said deep wells are formed to be continuous.

29. The method of claim 28 wherein said deep wells are continuous for at least 1.5 μm approximately from a surface of said substrate underneath said insulating layer.

30. The method of claim 26 wherein said deep wells are formed by ion implantation.

31. The method of claim 30 wherein said ion implantation comprises a first stage in which ions are accelerated to a first energy level and at least a second stage in which ions are accelerated to an energy level different from said first energy level.

32. The method of claim 31 wherein said first energy level in said first stage ranges approximately from 500 to 800 Kev and said second energy level in said second stage ranges approximately from 200 to 350 Kev.

33. The method of claim 31 wherein said first energy level in said first stage ranges approximately from 600 to 1200 Kev; said second energy level in said second stage ranges approximately from 350 to 500 Kev; and a third energy level in a third stage ranges approximately from 150 to 250 Kev

34. A method of manufacturing an inductor on an integrated circuit, comprising:
providing a semiconductor substrate of a first conductivity type;
forming a shallow trench isolation region in a substrate;
forming at least two deep wells of opposite conductivity type in said substrate underneath said shallow trench isolation region;
forming an insulation layer over said substrate; and
forming a conductive trace over said insulating layer.

35. The method of claim 34 wherein said deep wells are arranged in a pattern to form a substantial depletion space in said substrate underneath said trace.

36. The method of claim 34 wherein said deep wells are formed to be continuous.

37. The method of claim 36 wherein said deep wells are continuous for at least 1.5 μm approximately from a plane in said substrate underneath and adjacent to said shallow trench isolation region.

38. The method of claim 34 wherein said deep wells are formed by ion implantation.

39. The method of claim 38 wherein said ion implantation comprises a first stage in which ions are accelerated to a first energy level and at least a second stage in which ions are accelerated to an energy level different from said first energy level.

40. The method of claim 39 wherein said first energy level of said first stage ranges approximately from 500 to 800 Kev and said second energy level of said second stage ranges approximately from 200 to 350 Kev.

41. The method of claim 39 wherein said first energy level of said first stage ranges approximately from 600 to 1200 Kev; said second energy level of said second stage ranges approximately from 350 to 500 Kev, and a third energy level of a third stage ranges approximately from 150 to 250 Kev.